

COURSE INFORMATION

Spring 2009

EGR 270

Fundamentals of Computer Engineering

Pre-requisites: EGR 260, EGR 125

Co-requisite: none

Credits: 4

Lecture Hours: 3 hr/week

Lab Hours: 3 hr/week

Instructor: Paul Gordy

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Paul Gordy's Home Page - www.tcc.edu/faculty/webpages/PGordy/

Course Material:

1. **Lecture Notes/PowerPoint Presentations** - This is the primary source of information for this course. Material covered in lecture may not be found in the textbook. Students should print the PowerPoint presentations prior to class and use them to take notes as the presentations leave space for problems solved in class. If any lectures are missed, the student should try to copy the notes from another student.
2. **Textbook** - This course will follow the textbook somewhat closely. Reading assignments and problem assignments will generally be made from the textbook that will serve to reinforce concepts covered in the lectures. The textbook used in this course is: M. Moris Mano, Logic and Computer Design Fundamentals, 4th Edition, Upper Saddle River, NJ, Pearson Prentice-Hall, 2007 (ISBN: 978-0-13-600418-9)
3. **Optional PSPICE Textbook** - This additional text serves as a reference for PSPICE programming assignments made in EGR 260, 261, and 270. The text is Schematic Capture with Cadence PSPICE, 2nd Edition by Marc Herniter (ISBN: 9780130484000).

Course Description:

EGR 270 covers topics including the design and organization of digital systems including number systems, Boolean algebra, logic gates, Karnaugh maps, combinational and sequential logic circuits, timing diagrams, and synchronous and asynchronous controllers. Hardware description language (HDL) and assembly language programming will be introduced and concepts related to computer organization will be explored, including Register Transfer Language (RTL), Instruction Set Architecture (ISA) and Memory Controllers. EGR 270 includes a lab which will utilize design and modeling techniques introduced in class as well as expose the student to many practical issues concerning the constructing and testing digital circuits. Experiments include building circuits with logic gates; programming in Hardware Description Language (HDL) and implementing logic designs using programmable logic devices (PLDs); and programming in assembly language and testing the programs on 68HC11 microprocessors. The lab also covers the use of test equipment, report-writing techniques, and lab safety.

Grading:

Course grades will be computed based on the following percentages:

| | |
|----------------------------------|-----|
| 3 Tests (14% each) | 42% |
| Final Exam (comprehensive) | 17% |
| Homework Assignments (1 dropped) | 8% |
| PSPICE Assignments | 8% |
| Lab Grade (8 labs) | 25% |

Course Objectives:

- Represent numbers and perform arithmetic operations in various bases and convert between bases.
- Express, simplify, and minimize Boolean functions through various methods, including truth tables, Boolean algebra, and Karnaugh maps
- Implement logical expressions using defined logic functions.
- Analyze and synthesize combinational logic circuits
- Analyze and synthesize sequential logic circuits, including the use of state diagrams, state tables, excitation tables, and state equations.
- Implement logic circuits using Programmable Logic Devices (PLDs).
- Expose students to concepts in computer organization
- Simulate logic circuits and explore concepts in computer organization through the use of HDL and assembly language.
- Gain exposure to different logic families and types of commercial devices
- Gain practical knowledge in the construction and testing of digital circuits
- Gain experience in HDL programming, including the implementation and testing of designs
- Gain experience in assembly language programming and testing
- Develop report-writing techniques
- Gain exposure to the use of PLD programming software and hardware

Homework:

Reading and problem assignments will be made regularly. The problem assignments will be due on a specified date, but may or may not be collected for grading. Problem solutions will be handed out when the assignments are due. Late homework assignments are generally not accepted. The lowest homework grade of those collected will be dropped. Homework may include programming assignments in HDL and assembly language.

Homework Format - Each assigned homework problem must contain the complete problem statement including any associated diagrams, circuits, etc. If this requirement is not met, a minimum of 10 points (out of 100) will automatically be deducted from the homework grade or the assignment may not be accepted. Neatness and presentation will be a factor in the grade.

PSPICE Assignments:

Two assignments will be made using PSPICE, a circuit analysis program. PSPICE has a wide assortment of digital logic devices that can easily be used to implement designed circuits. Timing diagrams can be generated to verify circuit outputs. Students will design and verify both combinational and sequential logic circuits using PSPICE.

Absence:

A missed test or lab results in a grade of 0 unless the student notifies the instructor prior to class or within 24 hours of the class with an adequate reason. Notification may be made by phone or by email. If a class is missed it is the responsibility of the student to obtain any information, assignments, etc., given during class.

Lab:

The lab for the course will meet weekly and will include 8 laboratory experiments. Most labs will only require one lab period, but some will require two lab periods. Additionally, two lab periods will be used for tests (Test #1 and Test #2). More information on the lab portion of the course will be provided during the first lab meeting.

Tentative Course Outline:

- I. Digital Computers and Information (Chapter 1)
 - A. Digital systems
 - B. Number systems
 - C. Decimal and alphanumeric codes
- II. Combinational Logic Circuits (Chapter 2)
 - A. Boolean algebra
 - B. Logic gates & implementing logic expressions
 - C. Truth tables
 - D. Canonical forms and standard forms
 - E. Implicants, essential and prime
 - F. Reduction by Karnaugh maps (2-5 variable)
 - G. Product of Sums (POS) and Sum of Products (SOP) implementations
 - H. Don't care conditions
 - I. Multiple-level circuit implementation
 - J. Additional logic gates

TEST #1 (Chapters 1 - 2)

- III. Combinational Logic Design (Chapter 3)
 - A. Design procedure
 - B. Hierarchical design
 - C. Verification
 - D. Technology mapping (Ex: NAND and NOR implementations)
 - E. Rudimentary Logic Functions
 - F. Decoders and enabling
 - G. Encoders, priority encoders, and multiplexers
 - H. Implementing combinational logic functions using decoders and multiplexers
- IV. Arithmetic Functions and Circuits (Chapter 4)
 - A. Binary addition, subtraction, and multiplication
 - B. Other arithmetic functions
 - C. Hardware Description Language (HDL) for combinational logic circuits

TEST #2 (Chapters 3 - 4)

- V. Sequential Circuits (Chapter 5)
 - A. Flip-flops and latches
 - B. Sequential circuit analysis
 - C. Mealy models and Moore models
 - D. State diagrams and state tables
 - E. Sequential circuit timing
 - F. Design of sequential circuits
 - H. Hardware Description Language (HDL) for sequential circuits
- VI. Selected Design Topics (Chapter 6)
 - A. The Design Space
 - B. Gate propagation delay
 - C. Flip-flop timing and sequential circuit timing
 - D. ROM and programmable logic devices (PLDs)
- VII. Registers and Counters (Chapter 7)
 - A. Registers and register operations
 - B. Synchronous and ripple counters
 - C. Asynchronous counters versus synchronous counters

TEST #3 (Chapters 5 - 7) – Take-home test

- VIII. Assembly Language (Chapter 10, handouts, notes)
 - A. Assembly language and computer architecture
 - B. Instruction sets and addressing modes
 - C. 68HC11
 - D. Programming concepts
- IX. Memory (Chapter 8)
 - A. Tri-state devices
 - B. Random Access Memory (RAM)

FINAL EXAM (Comprehensive)

Lab Grading

- The lab grade makes up 25% of the course grade for EGR 270.
- All labs require verification of proper circuit operation by the instructor.
- Lab reports will not be accepted until all circuits in the lab have been built and verified.
- The grade for the lab portion of EGR 270 is simply the average of the lab report grades.
- All labs require that a Preliminary Work section be completed before lab. The Preliminary Work will be briefly checked by the instructor and will affect the lab report grade as follows:
 - Preliminary Work completely done – full credit on lab report
 - No Preliminary Work done: deduct 10 points from lab report grade
 - Preliminary Work partially done: deduct 1 to 9 points from lab report
- Note that the Preliminary Work will also be graded for accuracy and completeness when it is submitted as part of the lab report.

Tentative Schedule

| Date | Topic |
|-------------|--|
| Jan 13 | No class |
| Jan 20 | Introduction to lab equipment, course procedures, etc. |
| Jan 27 | Lab #1: Introduction to Logic Circuits |
| Feb 3 | Lab #2: Characteristics of TTL gates |
| Feb 10 | Test 1 or Lab #2 continued (if necessary) |
| Feb 17 | Test 1 or Lab #2 continued (if necessary) |
| Feb 24 | Lab #3: Combinational Logic Circuits |
| Mar 3 | Lab #4: 7-segment displays, decoders, and multiplexers |
| Mar 10 | TCC Closed – Spring Break |
| Mar 17 | Lab #5 VHDL Combinational Logic Circuit |
| Mar 24 | Test 2 or Lab #5 continued (if necessary) |
| Mar 31 | Test 2 or Lab #5 continued (if necessary) |
| Apr 7 | Lab #6: Sequential Counters |
| Apr 14 | Lab #7: VHDL Sequential Logic Circuit |
| Apr 21 | Lab #8: Assembly language/MicroStamp11 |
| Apr 28 | Lab #8 continued (if necessary) |

Lab Policies

- Each lab session will begin with a lecture by the instructor on the following lab. Attendance for the lectures is critical as new material is introduced in many of the labs.
- Students may work alone or with a partner on some of the labs. However, some labs require the design and/or implementation of customized circuits (on the EmplID, for example), so students must work alone on these labs.
- Each student must submit their own lab report for each lab.
- Lab reports are due on the date of the next lab. For example, Lab Report #2 is due on the day the class will be performing Lab #3.
- The key to each lab is proper verification of circuit operation. Therefore,
 - If you do not complete a lab during the class session, you can use the lab during open lab times and let the instructor know when you are ready to demonstrate each circuit.
 - If you miss a class (not advised), you can demonstrate each circuit whenever the instructor is available. Note that the instructor should be notified if a lab is to be missed so that other arrangements can be made.
 - If you would like to work ahead and reduce the amount of time spent in lab, you can work in the lab (or check out a breadboard and components) and demonstrate each circuit whenever the instructor is available.

General Information

TCC College and Student Handbook

Students are responsible for being aware of the policies, procedures, and student responsibilities contained within the current edition of the Tidewater Community College Catalog and Student Handbook. Students should familiarize themselves with the College's policies regarding misconduct and inclement weather policies found in the Student Handbook.

Last Day to Withdraw Without Academic Penalty

You may withdraw from a course without academic penalty during the first 60% of a session and receive a grade of "W"(withdrawal). The last day to withdraw without academic penalty is **March 20, 2009**. After that date, the student will receive a failing grade of "F" or "U". Exceptions to this policy may be made ONLY when initiated by the instructor and approved by the division dean; ONLY if you are able to document mitigating circumstances; and ONLY if you were making satisfactory progress in the course. **Students are advised to discuss attendance irregularities with the instructor. Do not simply stop attending. Failure to properly complete the withdrawal procedure may result in the assignment of "F" or "U" grades to your permanent record.**

Disability Services Statement

Disabilities Services of Tidewater Community College provides students, faculty, and staff programmatic and physical access in a supportive atmosphere and in accordance with Section 504 of the 1973 Rehabilitation Act and the Americans with Disabilities Act of 1990. In appreciation of the unique talents and needs of students with disabilities and chronic health issues, Disabilities Services further provides an array of services designed to enhance all educational experiences. *Students with disabilities or chronic health problems are encouraged to identify themselves to a Disability Services [DS] Counselor as early as possible. DS Counselors are on all campuses. Students with documented disabilities may qualify for academic accommodations such as more time on tests, sign language interpreting or Braille.*

Emergency Procedures

In the event of a bomb threat, tornado, or fire, students and staff may be asked to evacuate the building or move to a secure location within the building. Evacuation routes for movement to an external location or to a shelter within the building are posted at the front of the room. Students should review the maps and make sure that the exit route and assembly location for the building are clearly understood. If you have a disability that may require assistance during an evacuation, please let your faculty know at the end of the first class.

Cheating

College rules state that a student may be subjected to disciplinary action for academic cheating, plagiarism, or assisting in cheating or plagiarism. Disciplinary penalties include college dismissal or suspension. In addition, cheating, plagiarism, or assisting such activity is a most serious form of academic misconduct, and will in the sole discretion of the faculty member result in a grade of F on the work or for the course. A single act of cheating may subject a student to both a failing grade in the course, and student disciplinary action perhaps involving suspension or dismissal from TCC.