EGR 270 Due date: See Due Dates Table
Fundamentals of Computer Engineering
File: N270H3

Homework Assignment #3

Reading Assignment:

Chapter 3 in the textbook Logic and Computer Design Fundamentals, 4th Edition by Mano

Problem Assignment:

1) Chapter 3 problems: 1, 2, 3, 4, 6, 8, 9, 16, 17, 20, 29, 35, 36, 37, 40, 44, 46, 47, 48
   Hint for 3-6: The light should turn on when an odd number of switches are in the ON position.
2) A combinational logic circuit has 3 outputs as described below:

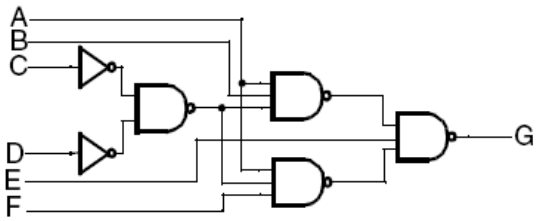
$$F_1 = \Sigma(0,3,4) \quad F_2 = \Sigma(1,2,7) \quad F_3 = \Pi(0,1,2,4)$$

   A) Implement the circuit using a single decoder with active-HIGH outputs and external 2-input OR gates
   B) Implement the circuit using a single decoder with active-LOW outputs and external 2-input AND gates
3) Design a driver circuit for a common-anode 7-segment display that operates as follows:
   - The display should show 0-5 for the corresponding BCD inputs
   - The display should be blank for inputs 6 – 15
   - Recall that a LOW output is required to light a segment on a common-anode display
   - Show the truth table, the Kmaps used to determine the 7 output expressions (minimal SOP), and the logic diagram.

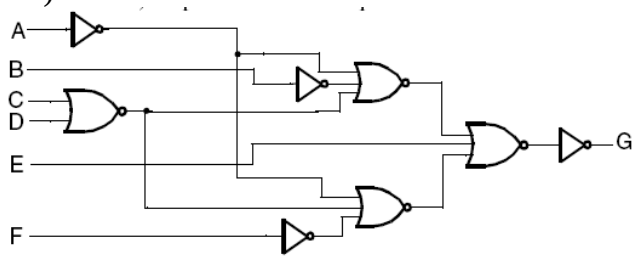
Selected Answers:

3-1) F = XZ + XY + YZ
3-3) F = AB + AC
3-4) W=ABC'D'+AB'CD, X=A'BCD+AB'C'+AB'D', Y=(A⊕B)(C⊕D), Z=A'BD'+BC'D'+AB'D'
3-6) Z = X1⊕X2⊕X3
3-8) S0 = C, S1 = 0, S2 = A'BC' + ABC', S3 = A'BC + AB'C, S4 = AB' + AC, S5 = AB
3-9) S0 = B'C'D+B'CD'+AB'+AC'D'+A'BCD, S1 = A'B+AB'+A'CD+BC'D', S3 = ABC+ABD

3-16)

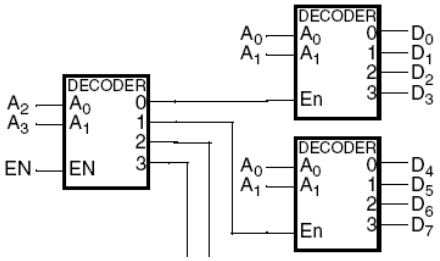


3-17)



3-20) Algebraically show that F = XY + X'Y'

3-29) (partial diagram)

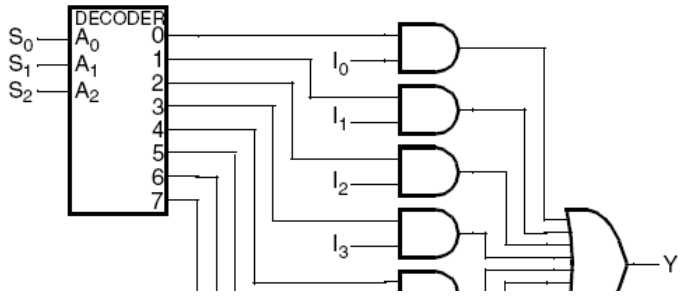


3-36) (partial truth table)

Decimal Inputs										Binary Outputs				
9	8	7	6	5	4	3	2	1	0	A_3	A_2	A_1	A_0	V
0	0	0	0	0	0	0	0	0	0	X	X	X	X	0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	0	1	X	0	0	0	1	1

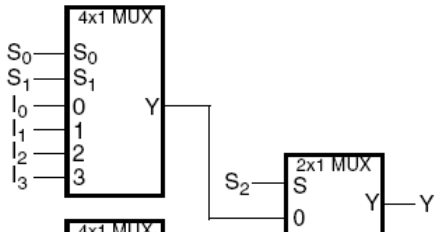
3-37) (partial diagram)

a)

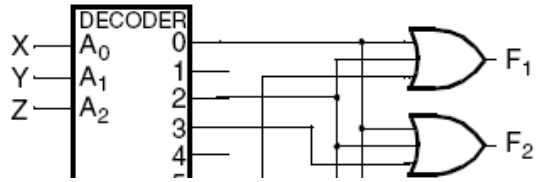


3-40) (partial diagram)

b)



3-44) (partial diagram)

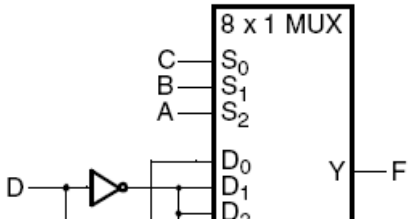


3-46) (partial mux table and diagram)

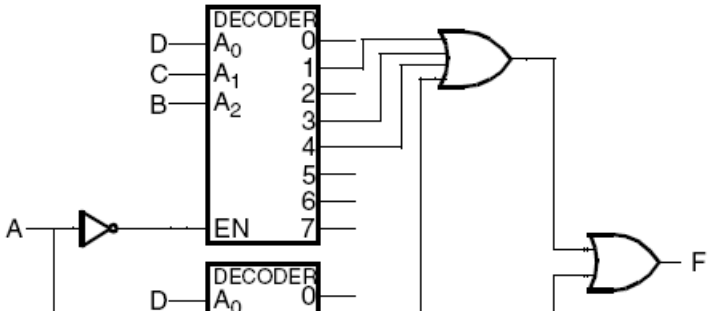
A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0

$F = 0$

$F = \overline{D}$



3-48) (partial diagram)



2A) To generate F1, OR decoder outputs D0, D3, and D4. Similar approach for F2 and F3.

2B) To generate F1, AND decoder outputs D1, D2, D5, D6, and D7

3) a = A + BC + BD' + B'C'D

b = A + BC + BD

c = A + BC + CD'

etc