

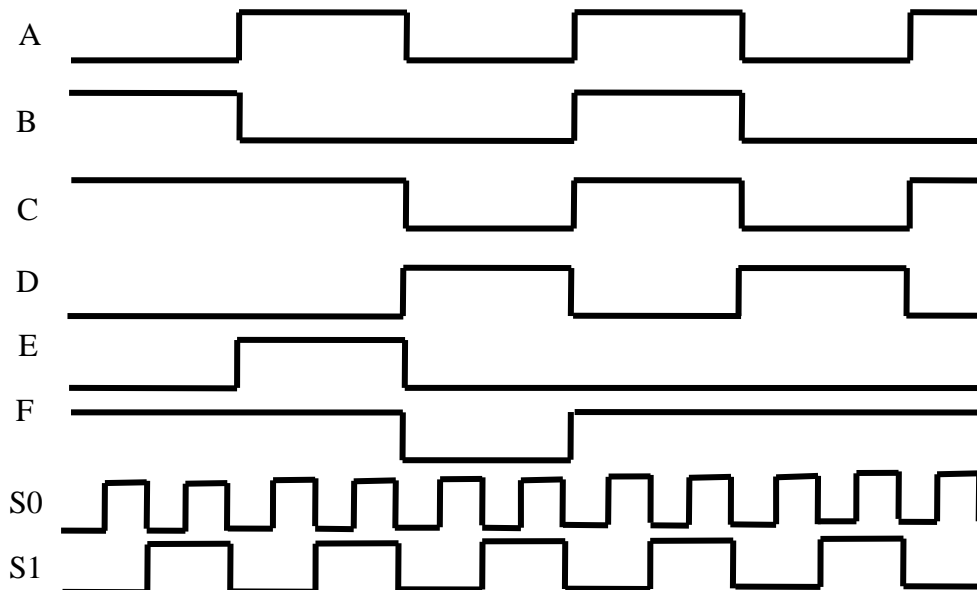
Homework Assignment #4

Reading Assignment:

Chapters 3-4 in the textbook Logic and Computer Design Fundamentals, 4th Edition by Mano

Problem Assignment:

- 1) Chapter 4 problems: 2, 3, 4, 5, 6, 7, 9, 16
- 2) A) Implement a full-adder using a PAL like the one shown on page 17 of the Lecture 8 notes. The inputs should be labeled A, B, and C_i . The outputs should be labeled S and C_o . Print page 17, label the inputs and outputs, and use X's to show all the connections required in the PAL.
B) Implement a 2x1 multiplexer using a PLA like the one shown on page 15 of the Lecture 8 notes. The inputs should be labeled I0, I1, and S, where S is the select line. The output should be labeled Y. Print page 15, label the inputs and outputs, and use X's to show all the connections required in the PLA.
- 3) Timing Diagrams: Using the input waveforms below, sketch the outputs described in each part below. Show the inputs as well as the outputs in each case so that it is clear where each transition occurs.
 - A. Sketch the output $F_2 = AB + AC + BC$ using the input waveforms A, B, and C shown below.
 - B. If a 3-bit magnitude comparator has inputs $P = ABC$ and $Q = DEF$ (A and D are the MSBs) using the waveforms A-F below, sketch the 3 outputs of the comparator.
 - C. If A, B, C, and D are the input lines to a 4 x 1 multiplexer (A = input 0), and S1, S0 are the select lines, sketch the output Y.
 - D. If A, B, and C are the inputs to a 3-line-to-8-line decoder, sketch the outputs D0, D5, and D7 if:
 - 1) waveform E is an active LOW enable and the outputs are active LOW
 - 2) waveform F is an active HIGH enable and the outputs are active HIGH



- 4) Write the VHDL code (entity and architecture) for each problem below:
 - A) A 4-bit prime number indicator with inputs A,B,C,D and output P where $P=1$ when the input ABCD is a prime number.
 - B) An Excess-3 to BCD code converter as described in textbook problem 3-12.
 - C) A 3-bit squaring circuit as described in textbook problem 3-15.

- 5) Draw the circuit and determine the output for the VHDL code in each part below.
- A) Draw the circuit corresponding to the following VHDL code and then use a K-map to express the output $F(W,X,Y,Z)$ as a sum of minterms:

```

library IEEE;
use IEEE.STD_LOGIC_1164.all;
entity Problem5A is
    port(
        W,X,Y,Z : in STD_LOGIC;
        F : out STD_LOGIC);
end Problem5A;
architecture Problem5A of Problem5A is
begin
    F <= (X and Z) or ((not W) and X and (not Y)) or (W and X and
        Y) or ((not W) and Y and Z) or (W and (not Y) and Z);
end Problem5A;

```

- B) Draw the circuit corresponding to the following VHDL code and then use a K-map to express the output $F(A,B,C,D,E)$ as a sum of minterms:

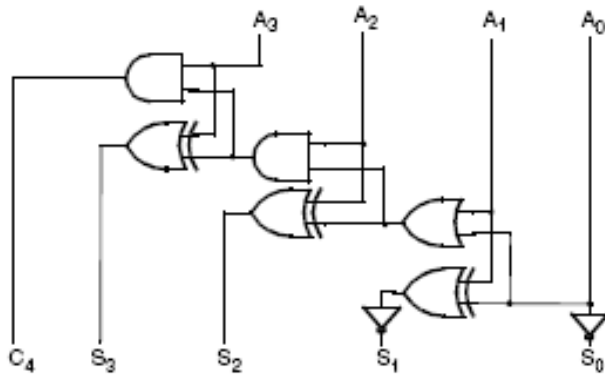
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library IEEE;
use IEEE.STD_LOGIC_1164.all;
entity Problem5B is
    port(
        A,B,C,D,E : in STD_LOGIC;
        F : out STD_LOGIC);
end Problem5B;
architecture Problem5B of Problem5B is
begin
    F <= (((not A) nand B) and D) or (C nor D) or (C xor E);
end Problem5B;

```

Selected Answers:

- 4.2) $C_1 = A_0B_0 + A_0C_0 + B_0C_0$, $S_0 = A_0 \oplus B_0 \oplus C_0$
 4.4) a) 01001 b) 10000 (= -10000) c) 0000000 d) 100100 (= -011100)
 4.5) a) 01001 b) 00000 c) 0000000 d) 101100
 4.6) (check the results by converting the results back to decimal)
 4.7) a) 100000 (-32) b) 110001 (-15) c) 011111 (-33) overflow d) 110111 (-9)
 4.9)



4.16) (3 of 5 parts shown)

	S	A	B	C ₄	S ₃	S ₂	S ₁	S ₀
a)	0	0111	0111	0	1	1	1	0
b)	1	0100	0111	0	1	1	0	1
c)	1	1101	1010	1	0	0	1	1