

Lab # 2

Logic Gate Characteristics

A. Objectives

The objectives of this laboratory are:

- To become familiar with data sheets for logic gates
- To investigate various logic gate characteristics, including voltage and current levels, loading (fanout), and propagation delay.
- To become familiar with the difference between logic gates with totem-pole outputs and open-collector outputs.
- To investigate the uses of open-collector gates
- To use open-collector gates to provide higher output voltage levels
- To use open-collector gates and output transistors to provide high current levels for loads

B. Materials

Breadboard

Tektronix P5280 DC Power Supply

Agilent 33120A Function Generator

Tektronix TDS 2002 Digital Storage Oscilloscope

Agilent 33401A Digital Multimeter (Two)

Micronta Digital Logic Probe

7400 Quad 2-input NAND IC (totem-pole outputs)

7401 Quad 2-input NAND IC (open-collector outputs)

7406 or 7416 Hex Inverter Buffer/Driver (open collector)

TIP30C PNP transistor ($I_C(\text{max}) = 3\text{A}$)

12V Automobile Marker Bulb (#194)

12V DC Motor (12,500 rpm)

Handout: "**Downloading Data Sheets from the Internet**"

C. Introduction

The physical characteristics of logic gates often play an important role in the design of digital circuits. This lab focuses on several of these characteristics, including:

- voltage and current levels
- noise margin
- fanout and loading
- propagation delay

Each of these physical characteristics are discussed below.

Current Direction: According to IEEE standards, *currents are directed into devices*. Therefore, if a current in a specification is positive, it is entering the device. If a current in a specification is negative, it is leaving the device.

Voltage and Current Levels

Several voltage and current levels are of interest when working with logic gates, including:

V_{OL} = output voltage when the gate is LOW

V_{OH} = output voltage when the gate is HIGH

V_{IL} = input voltage when the gate is LOW

V_{IH} = input voltage when the gate is HIGH

I_{OL} = output current when the gate is LOW

I_{OH} = output current when the gate is HIGH

I_{IL} = input current when the gate is LOW

I_{IH} = input current when the gate is HIGH

The voltages defined above have fixed values for TTL devices. Check the specification sheet for the 7400 NAND during lecture and record the values indicated in the table shown below.

Specification	7400 NAND
$V_{CC}(\text{min})$	
$V_{CC}(\text{max})$	
$V_{IL}(\text{max})$	
$V_{IH}(\text{min})$	
$V_{OL}(\text{max})$	
$V_{OH}(\text{min})$	
$I_{IL}(\text{max})$	
$I_{IH}(\text{max})$	
$I_{OL}(\text{max})$	
$I_{OH}(\text{max})$	
$t_{PLH}(\text{max})$	
$t_{PHL}(\text{max})$	

Noise Margins

$V_{OL}(\text{max})$ is lower than $V_{IL}(\text{max})$ to allow for noise and signal deterioration. Similarly $V_{OH}(\text{min})$ is higher than $V_{IH}(\text{min})$. These differences in voltages are referred to as *noise margins*. Defined more exactly:

$$V_{NL} = \text{LOW level noise margin} = V_{IL}(\text{max}) - V_{OL}(\text{max})$$

$$V_{NH} = \text{HIGH level noise margin} = V_{OH}(\text{min}) - V_{IH}(\text{min})$$

For standard TTL devices:

$$V_{NL} = 0.8 \text{ V} - 0.4 \text{ V} = 0.4 \text{ V}$$

$$V_{NH} = 2.4 \text{ V} - 2.0 \text{ V} = 0.4 \text{ V}$$

These TTL noise margins are illustrated in Figure 1 below:

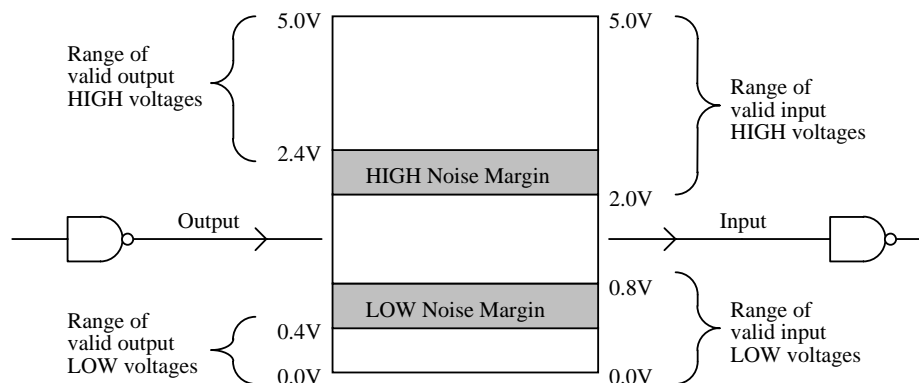


Figure 1: Noise Margins

Fanout

Fanout is the number of standard loads that the output can drive. The number of standard loads is limited by the amount of input current each load requires as compared to the current that the driving gate can deliver. Fanout, therefore, is generally considered to be the smaller of the following two items:

$$\text{fanout} = \frac{I_{OL}(\text{max})}{I_{IL}(\text{max})} \quad \text{or} \quad \text{fanout} = \frac{I_{OH}(\text{max})}{I_{IH}(\text{max})}$$

Fanout is 10 for standard TTL devices. This is illustrated in Figure 2 below using 7400 NANDs (with their inputs tied together to act as inverters) where the output of the driving gate is LOW. Note that $I_{OL}(\text{max})$ is -16 mA and $I_{IL}(\text{max}) = -1.6 \text{ mA}$.

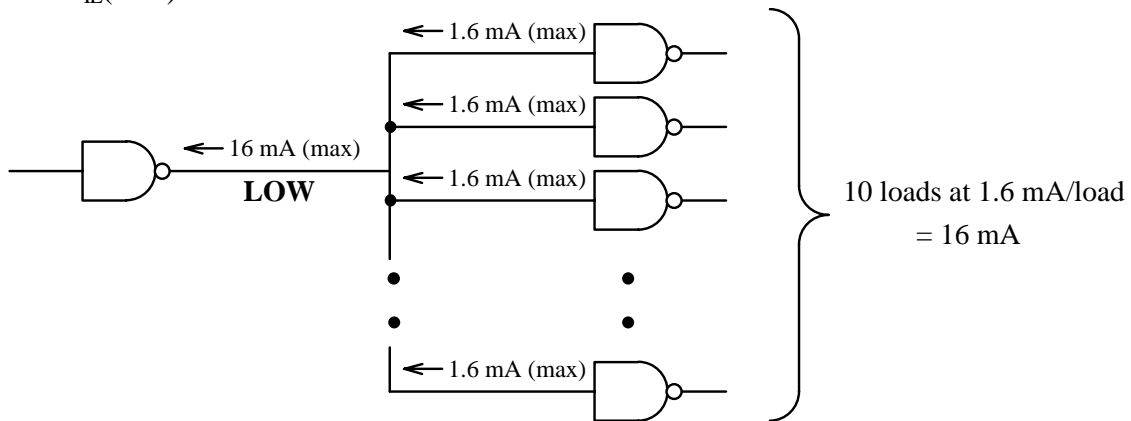


Figure 2: Fanout illustrated for a LOW TTL output driving 10 loads

Note that $I_{IL}(\text{max}) = -1.6 \text{ mA}$, but a typical value would be significantly less, so a fanout of 10 is a conservative estimate. A given circuit might be able to drive more actual loads than 10 without exceeding max values for I_{OL} or I_{OH} .

Propagation Delay

Propagation delay is the time that it takes a gate to switch logic levels. Logic gates often have a different propagation delay switching from LOW to HIGH than from HIGH to LOW, so two types of delay are defined:

t_{PLH} = propagation delay when the **OUTPUT** switches from LOW to HIGH

t_{PHL} = propagation delay when the **OUTPUT** switches from HIGH to LOW

An illustration of each type of propagation delay is shown in Figure 3 below.

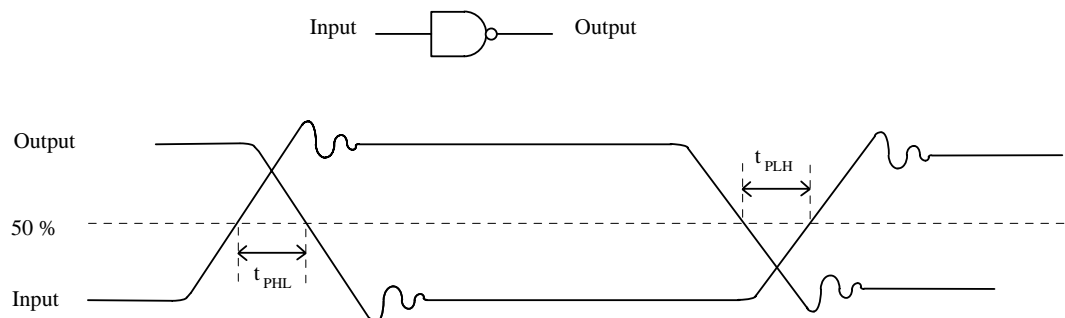


Figure 3: Propagation delay illustration

TTL logic circuits typically have one of two types of outputs:

- Totem-pole outputs
- Open-collector outputs

Totem-pole outputs

This is the most common type of output for TTL devices. Figure 1a below shows the internal circuitry of a 7400 2-input NAND. The transistors in TTL devices (denoted by Q) essentially act like switches. When a transistor is ON it acts like a closed switch and when a transistor is OFF it acts like an open switch. Note that transistor Q₄ is stacked on top of Q₃ like a totem-pole. The output Y is taken from the top of Q₃. Figure 1b shows the current path through the totem-pole when the output is HIGH and also when it is LOW.

When the output is HIGH: Q₄ is ON, Q₃ is OFF, and the current I_{OH} flows through Q₄ and out Y. Note that I_{OH} = 0.4 mA maximum.

When the output is LOW: Q₄ is OFF, Q₃ is ON, and the current I_{OL} flows in Y and through Q₃ to ground. Note that I_{OL} = 1.6 mA maximum.

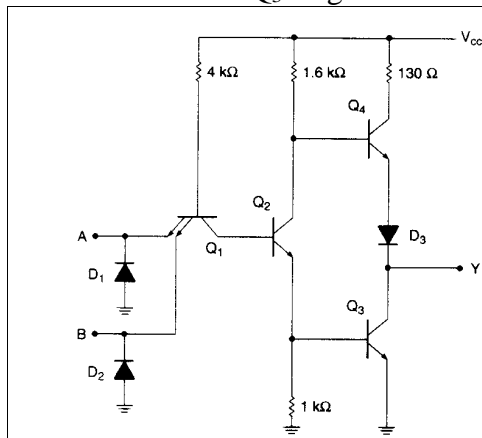


Figure 4A - 7400 NAND circuit

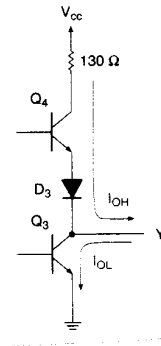


Figure 4B - current paths

Open-collector outputs

TTL circuits with open-collector outputs have only the lower transistor (Q₃) seen in the previous totem-pole output. Since there is no internal path from the output Y to the supply voltage V_{CC}, the circuit does not function properly unless an **external pull-up resistor** is used. Figure 5a below shows the internal circuitry of a 7401 open-collector 2-input NAND. Figure 5b shows a 7401 NAND with an external pull-up resistor attached.

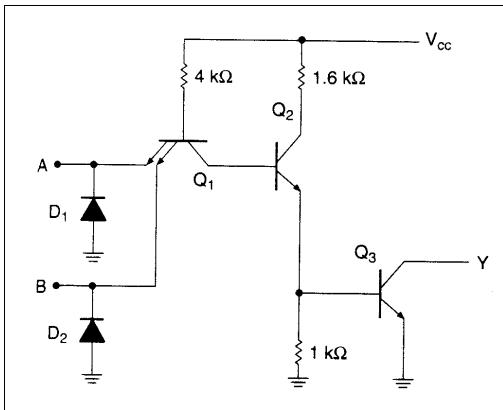


Figure 5a - 7401 open-collector NAND

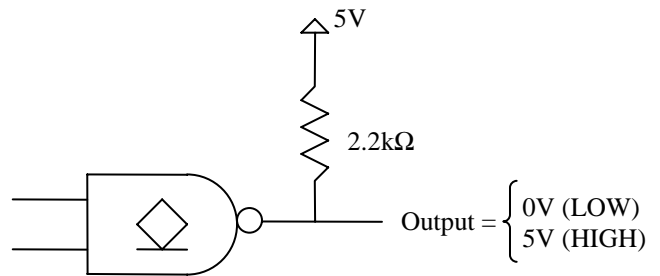


Figure 5b - 7401 NAND with pull-up resistor

Note that a special symbol is shown inside the NAND gate shown above. Open-collector gates are not always denoted with special symbols, but they may be indicated using one of the four symbols shown in Figure 6 below.

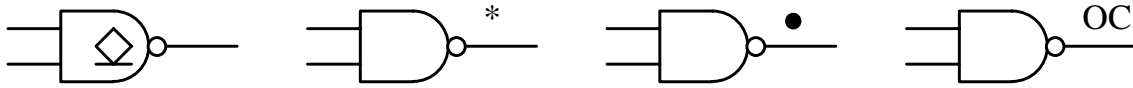


Figure 6 - Symbols for open-collector gates

Why should we use open-collector gates which require the addition of a pull-up resistor in order to function properly when we could use a gate with a totem-pole output instead? There are several reasons:

- 1) **Wired-ANDing** - Open-collector outputs can be tied directly together which results in the logical ANDing of the outputs. Thus the equivalent of an AND gate can be formed by simply connecting the outputs. This is especially convenient when large numbers of signals need to be ANDed. (Note that connecting the outputs of totem-pole gates will typically destroy them.)
- 2) **Increased current levels** - Standard TTL gates with totem-pole outputs can only provide a HIGH current output of 0.4 mA and a LOW current of 1.6 mA. Many open-collector gates have increased current ratings.
- 3) **Different voltage levels** - A wide variety of output HIGH voltages can be achieved using open-collector gates. This is useful in interfacing different logic families that have different voltage and current level requirements.

Providing different voltage levels with open-collector gates

Providing different HIGH voltage levels with open-collector gates is simply a matter of pulling the output up to the desired value using an external voltage source as illustrated in Figure 7 below.

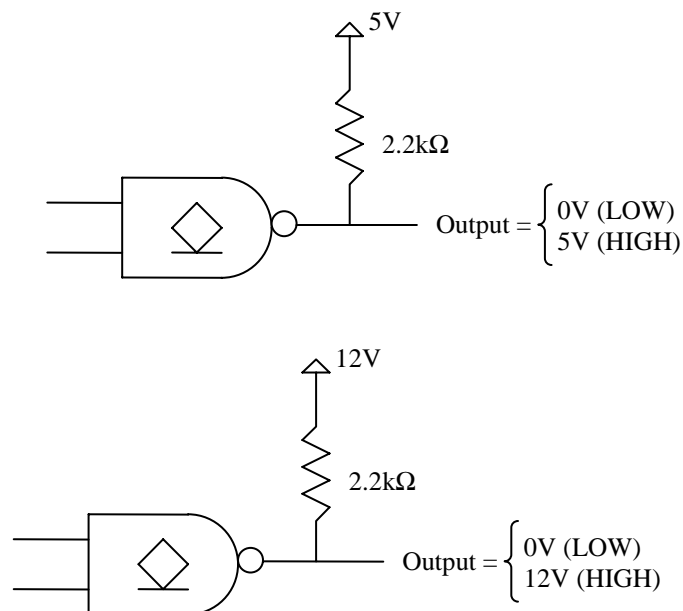


Figure 7: Open-collector gates with 5V and 12V outputs

Pull-up resistor calculation

Pull-up resistors are typically in the range of several hundred ohms to several thousand ohms, but exact ranges can be calculated using the relationships shown in Figures 8 and 9 below.

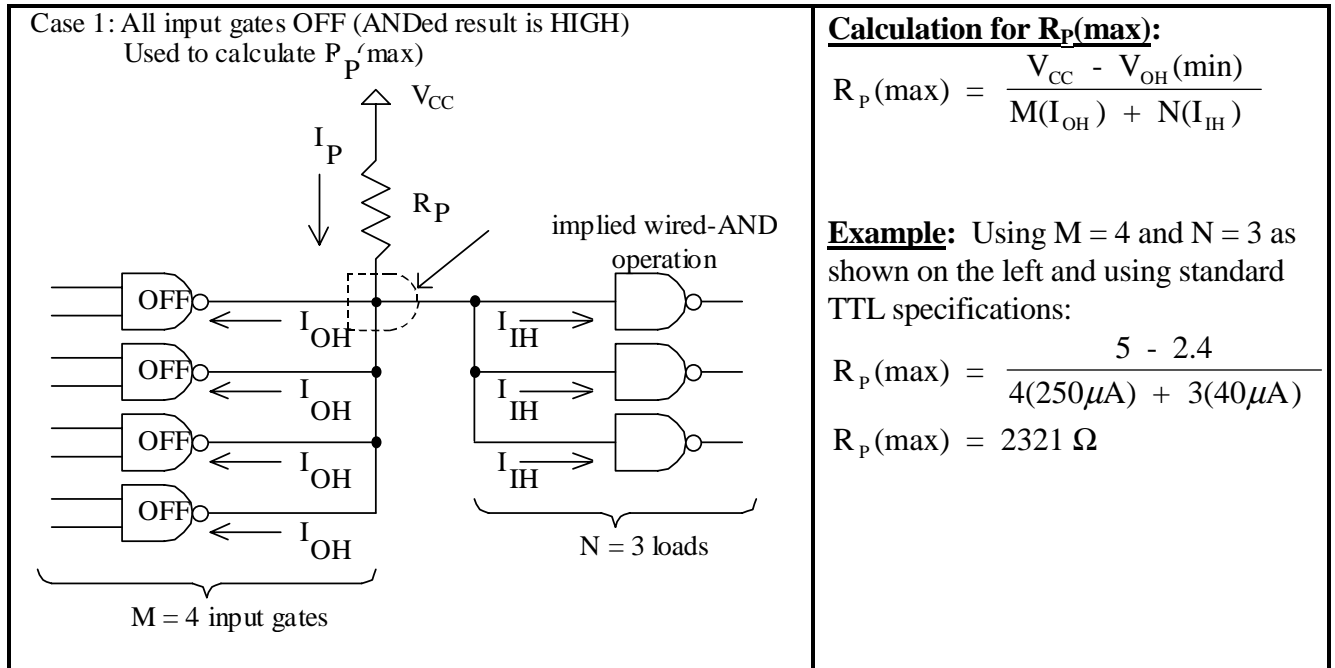


Figure 8 - Calculating the maximum pull-up resistor value

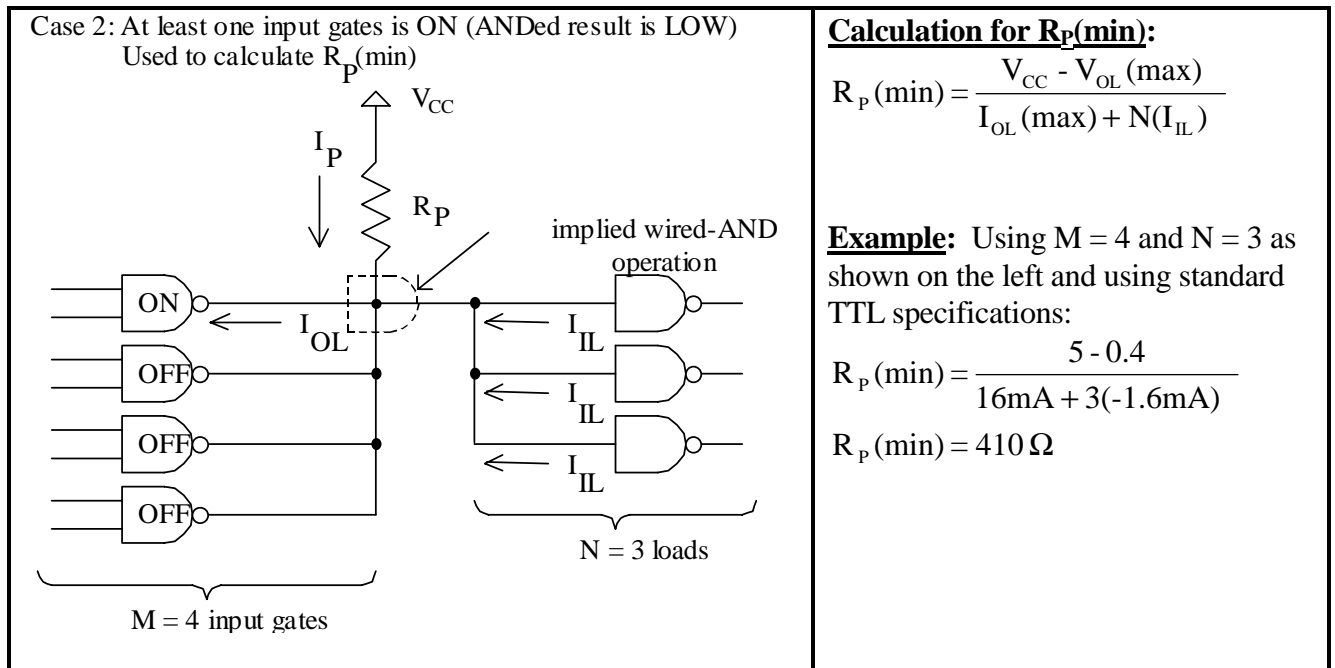


Figure 9 - Calculating the minimum pull-up resistor value

Open-collector drivers

Some open-collector gates are particularly well suited to driving loads that require higher voltage and current levels, such as incandescent lamps and relays. An example is the 7406 Hex Inverter Buffer/Driver. This gate is similar to the 7404 Hex Inverter (totem-pole output) except that $I_{OL}(\text{max}) = 40 \text{ mA}$ (instead of 16 mA) and $V_{OH}(\text{max}) = 30 \text{ V}$ (instead of around 5V). The term “driver” typically indicates that a device provides higher output currents.

An example is shown in Figure 10 below where the output of a 7406 is used to drive an incandescent lamp that requires a 12 V supply and about 35 mA of current. Note that a current-limiting resistor R_{limit} may or may not be necessary, depending on the resistance of the lamp filament.

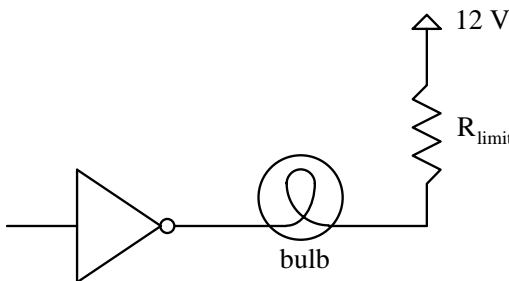


Figure 10 - 7406 driving an incandescent lamp

The 7406 allows us to drive loads that require up to 40 mA of current. For even larger currents, it may be necessary to use an output transistor. Transistors are available that can provide currents of several amperes. An example is shown in Figure 11 where a PNP power transistor is used to supply a current of 1A or more to a 12V DC motor.

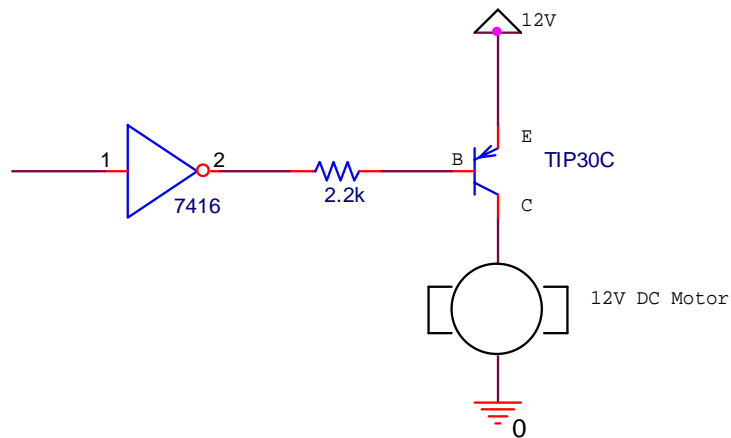


Figure 11 - Using an output transistor to provide large output currents

D. Preliminary Work

- Calculate minimum and maximum values for pull-up resistors under the following conditions. Use specifications for the 7401 (assume that $V_{OH(min)} = 2.4V$). Tabulate your results. Show a sample calculation for one case.

M (# inputs)	N (# outputs)
1	0
1	1
1	3
3	1
3	3

- Refer to the data sheet for the 7400, 74LS00, and 74S00 and complete the table shown below.

Specification	7400	74LS00	74S00
$V_{CC(min)}$			
$V_{CC(max)}$			
$V_{IL(max)}$			
$V_{IH(min)}$			
$V_{OL(max)}$			
$V_{OH(min)}$			
$I_{IL(max)}$			
$I_{IH(max)}$			
$I_{OL(max)}$			
$I_{OH(max)}$			
$t_{PLH(max)}$			
$t_{PHL(max)}$			
Fanout (min)			
V_{NL}			
V_{NH}			

- The 7404 is an inverter with totem-pole outputs. The 7406 and 7416 are inverters with open collector outputs. Refer to the data sheet for the 7404, 7406 and 7416. You can locate data sheets online by visiting Jameco Electronics (www.jameco.com)

Specification	7404	7406	7416
$V_{OH(max)}$			
$I_{OL(max)}$			
$I_{OH(max)}$			

E. Laboratory Work

1. Measurement of Voltages and Currents

- Fill out the specified values in table shown below using the 7400 data sheet. Include the word MIN or MAX with each specification.
- Construct Circuit 1 using a 7400 IC. (Note that a NAND gate with its inputs tied together acts like an inverter.)
- Apply a HIGH input to the first gate (thus the output is LOW) and measure the input current (I_{IL}) to the second gate and the output voltage (V_{OL}) of the first gate using a digital multimeter.
- Repeat the measurements with a LOW input to the first gate (thus the output is HIGH) and measure the input current (I_{IH}) to the second gate and the output voltage (V_{OH}) of the first gate.
- Record the results in the table below and verify that these values are within specified limits.

	Measured Value	Specified Value	Within Specs?
I_{IL}			
V_{OL}			
I_{IH}			
V_{OH}			

2. Logic Probes

Connecting the logic probe to HIGH or LOW points on a circuit will result in different colored LEDs lighting and different sounds from the probe.

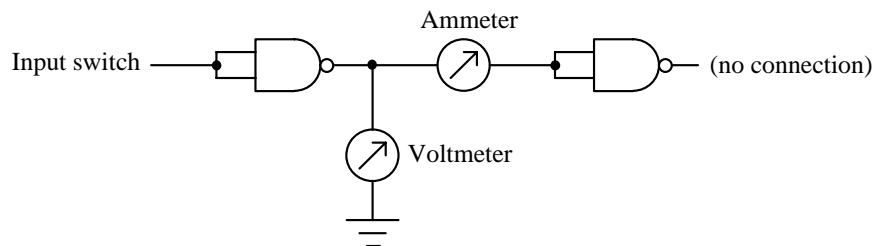
- Practice using a logic probe on Circuit 1 by checking a HIGH voltage (on pin 14) and a LOW voltage (on pin 7). Record the lights lit and sounds made in the table below.

Use Logic Probe to measure	Color LED lit	Sound made
HIGH Voltage (pin 14)		
LOW voltage (pin 7)		

- Next use a logic probe to check the inputs and outputs on an unused gate on the 7400 (no wires connected to the input or output, but powered up). Complete the table below.

Use Logic Probe to measure	Results (LOW, HIGH, or NO READING)
Open inputs	
Open output	

- Record the truth table for a 7400 NAND in your report. Highlight the line in the truth table that illustrates the only case where the output of the NAND is LOW.
- Based on the truth table above and your results using a logic probe on an unused gate, complete the following statement: Since the open output of the 7400 read _____, it can be stated that “OPEN INPUTS FOR 7400 SERIES GATES ACT LIKE _____.”



Circuit 1

3. **Propagation Delay Measurement** (Note: The instructor may set up this step as a demonstration. If so, be sure to get a printout of the waveforms showing t_{pHL} and t_{pLH} . Clearly label t_{pHL} and t_{pLH} exactly where they are measured on the printouts and label the input and the output.


- **Measure t_{pLH} :** Construct Circuit 2 shown below using the function generator and oscilloscope settings indicated below. Turn on the oscilloscope before turning on the computer and then run program **WaveStar for Oscilloscopes**. View both waveforms A and B on the oscilloscope and adjust the time scale until you can see t_{pLH} . Add two time cursors at the 50% points on waveforms and the difference between the cursors (also displayed) will be t_{pLH} . Capture the image with WaveStar and print it. Clearly label (by hand) where t_{pLH} is measured on the printed waveform. Also label the input and the output on the printout. Include the printout in your report.
- Repeat the step above to measure t_{pHL} .
- Compare the measured values to values found in the specification sheet (see table below).

Use the following settings for the function generator and the oscilloscope. (Note: Pressing AUTO SET on the oscilloscope will typically result in the correct settings!)

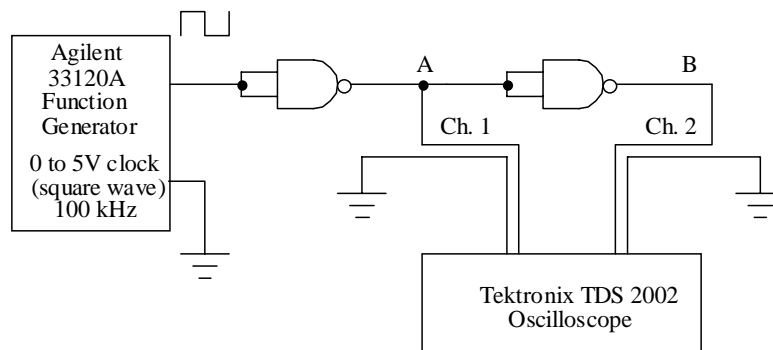
Tektronix TDS 2002 Oscilloscope

Control	Setting
Ch. 1/Ch. 2 Menu	Coupling: DC BW limit: OFF V/div: Coarse Probe: 1X Invert: Off
Trigger Menu	Type: Edge Source: Ch. 1 Slope: Rising Mode: Auto Coupling: DC
Ch.1 V/div	1V
Ch. 2 V/div	1V

Agilent 33120A Function Generator

Control	Setting
Function	 (square wave)
Frequency *	100 kHz
Amplitude *	5 Vpp
Offset *	2.5 Vpp

* Press the green "Enter Number" button and enter the specified value and the unit.

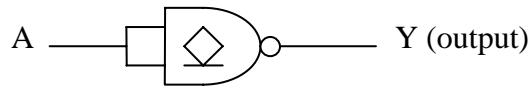


Circuit 2: Measurement of t_{pHL} and t_{pLH}

	Measured Value	Specified Value	Within Specs?
t_{pHL}			
t_{pLH}			

4. **Open-collector gate without a pull-up resistor**

- Connect a 7401 open-collector NAND with its inputs tied together (to act as an inverter) with no load and no pull-up resistor as shown in Circuit 3.
- Measure the output with a voltmeter for both HIGH and LOW inputs.
- Are both of the output voltages within specified ranges? (One should be out of specs.) Assume that $V_{OH(min)} = 2.4V$.

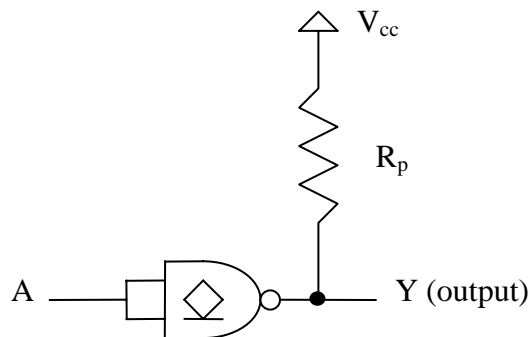


Circuit 3

Input Switch A	Output Voltage	Specified Voltage	Within specs?
L			
H			

5. **Open-collector gate with a pull-up resistor**

- Connect a 7401 open-collector NAND with its inputs tied together (to act as an inverter) and with no load using a pull-up resistor as shown in Circuit 4. Use $V_{cc} = 5V$.
- Use a pull-up resistor that is within the range calculated in the Preliminary Work.
- Measure the output with a voltmeter for both HIGH and LOW inputs.
- Are both of the output voltages within specified ranges? (They should be.) Assume that $V_{OH(min)} = 2.4V$.



Circuit 4

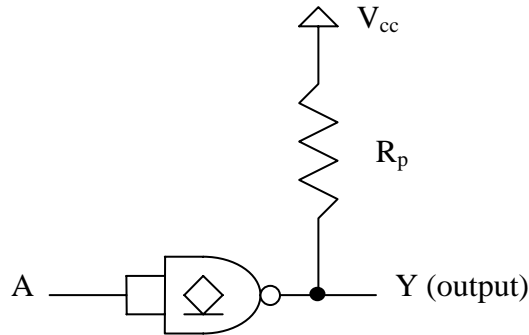
Input Switch A	Output Voltage	Specified Voltage	Within specs?
L			
H			

- Record the value of R_p used in the circuit above and compare it to $R_{P(min)}$ and $R_{P(max)}$ calculated in the Preliminary Work.

$R_{P(min)}$	
$R_{P(max)}$	
R_p – value used in Circuit 4 above	

6. **Open-collector gate with a pull-up resistor**

- Modify Circuit 4 used in the last step such that the pull-up resistor is connected to a 12V supply. **Warning: Connect the pull-up resistor to 12V, but be sure to power the 7401 using only 5V.**
- Measure the output with a voltmeter for both HIGH and LOW inputs.
- Are the results as expected?



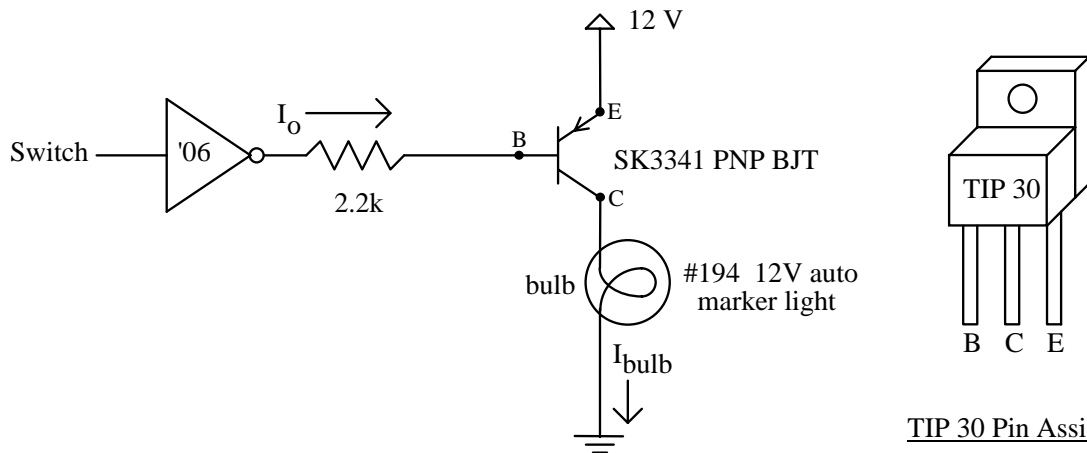
Circuit 4

Input Switch A	Output Voltage
L	
H	

7. **Driving an incandescent lamp using an output transistor**

- Connect Circuit 5 using either a 7406 or 7416 open-collector inverter. Use an SK3341, TIP30C, or equivalent PNP power transistor. **Warning: Connect 12V to the transistor, but be sure to power the 7406 using only 5V.**
- For both input switch positions, measure and record the 7406 current and voltage as well as the current through the bulb.

Input Switch A	V_o (7406)	I_o (7406)	I_{bulb}	Bulb lit?
L				
H				



TIP 30 Pin Assignment

Circuit 5

8. **Driving a 12V DC motor using an output transistor**

- Replace the bulb in Circuit 5 with a 12V DC motor and repeat the measurements.

Input Switch A	V_o (7406)	I_o (7406)	I_{motor}	Motor running?
L				
H				

Report

Remember that each lab report should have the following four sections:

Title Page**Preliminary Work**

- Include instructions

Lab Results

- Include all measured results. Use tables to summarize results whenever possible.
- Include step numbers and titles or headings that make it clear what is being shown.
- Include units whenever appropriate.

Discussion/Conclusion

- Discuss each part of the experiment performed in lab.
- Are the results as expected?
- What have you proven or demonstrated by completing the experiment?
- Explain any errors.
- Discuss in general when it would be appropriate to use open-collector gates and/or transistors.