

Lab # 5

Implementing Combinational Logic Circuits using PLDs

A. Objective

The objectives of this laboratory are to:

- introduce the student to Programmable Logic Devices (PLDs)
- introduce the student to basics of VHDL
- introduce the student to Aldec Active-HDL for designing and simulating combinational logic circuits and implementing the design into a Lattice GAL22V10 PLDs
- introduce the student to the CHIPMAX Universal Programmer for physically programming PLDs
- give the student an opportunity to design, program, and test a simple combinational logic circuit using a PLD

B. Materials

Breadboard

5V Power Supply

Wire, switches, etc.

GAL22V10 PLD

CHIPMAX Universal Programmer

Aldec Active-HDL Software

Common anode 7-segment display

Seven 220 Ω resistors

Handouts (available on instructor's web page):

“Combinational Logic Circuits Using Aldec Active-HDL”

“*GAL 22V10 Data Sheet*”

“*CHIPMAX Programmer Instructions*”

C. Introduction

Aldec Active-HDL - The handout “Combinational Logic Circuits Using Aldec Active-HDL” contains a detailed example on using Aldec Active-HDL to create a VHDL design and simulation that is to be implemented using a Lattice GAL 22V10 PLD.

GAL22V10

Programmable Logic Devices (PLDs) are programmable integrated circuits containing the equivalent of hundreds to millions of logic gates. The GAL22V10, produced by Lattice Semiconductor Corporation is a small PLD by modern standards, containing the equivalent of just a few hundred logic gates.

Lattice's GAL22V10 is a 24 pin E²CMOS PLD (electrically erasable (E²) programmable logic device) with the following features:

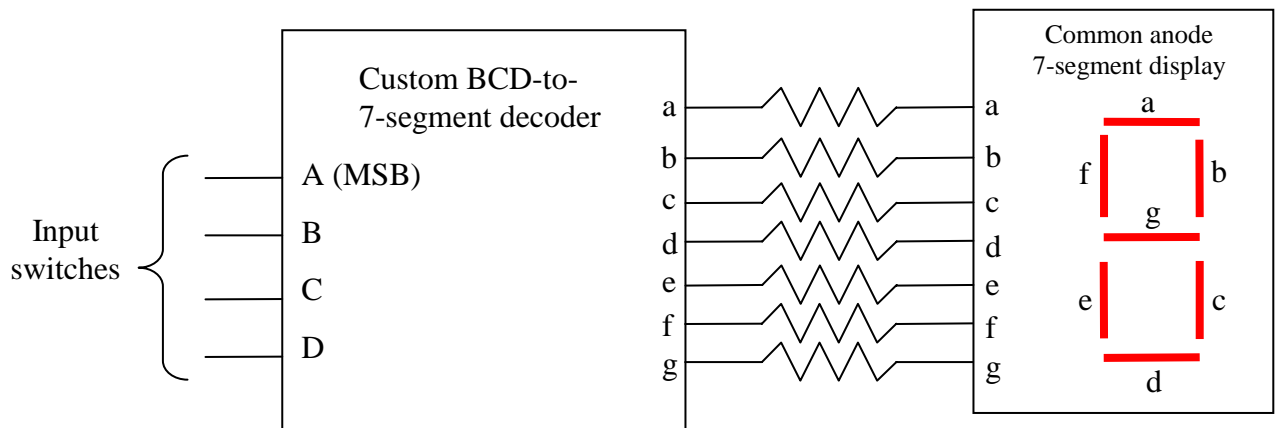
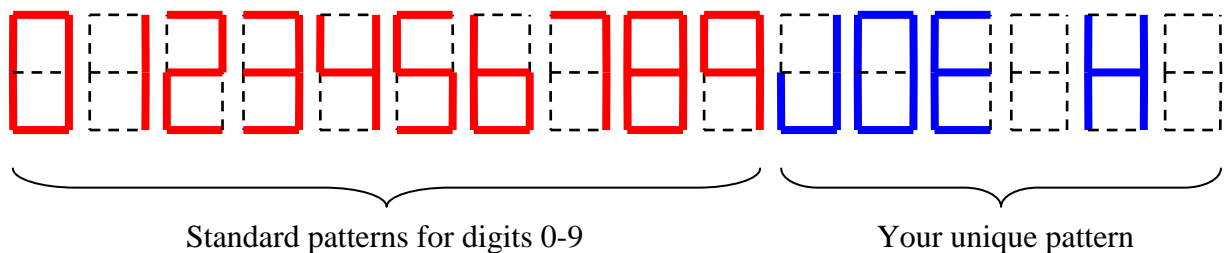
- Electrically erasable in under 100 ms
- 10 output logic macrocells (OLMC)
- Programmable architecture with up to 21 inputs or 10 outputs
- 4 ns propagation delay - counter frequencies up to 250 MHz
- 20 year retention of programmed data specified
- 100 erase/write cycles specified

GAL22V10 Pin Connections:

| Pin Connections | Pins Number/Notes |
|-------------------|---|
| Vcc | 24 |
| GND | 12 |
| Input or clock | 1 |
| Inputs only | 2-11, 13 |
| Outputs or inputs | 14 – 23 The number of product terms for outputs varies as follows: 14, 23 8 product terms 15, 22 10 product terms 16, 21 12 product terms 17, 20 14 product terms 18, 19 16 product terms |

D. Preliminary Work

- Design a custom BCD-to-7-segment decoder circuit as pictured below that will have the following features:
 - The output will be connected to a common-anode 7-segment display, so remember that a 0 (LOW) lights each segment.
 - Inputs 0-9 should light the usual segments for those digits.
 - Inputs 10-15 should light your name or initials as you would like them to appear (each student must have a unique pattern). Do not use any don't cares. An example is shown below. Clearly show which segments you will light for all BCD input combinations 0-15.
 - Include a truth table.
 - Include Karnaugh maps for the 7 outputs and determine a minimal SOP expression for each output.



2. Draw a logic diagram for the SOP circuit above using only AND gates, OR gates, and inverters. Assume that ANDs and ORs are available with any number of inputs. How many gates are required?
3. Generate **full circuit documentation** for the PLD circuit to be tested in lab. Leave off the pin numbers for the PLD inputs and outputs and add them later once they have been determined by the Aldec software. In addition to the PLD, include the 4-input switches, the 7-segment display, and the resistors.

E. **Laboratory Work**

1. Use Aldec Active-HDL to:
 - Use VHDL to define your custom BCD-to-7-segment decoder circuit.
 - Generate a testbench to test all 7 outputs for the 16 input combinations. Check to be sure that all outputs are correct for all input combinations before continuing.
 - Implement the design into a GAL22V10 PLD.
2. Program the GAL22V10 using the ChipMAX Universal Programmer. Take care in handling the PLD as it can be easily destroyed by static electricity.
3. Check the ChipReport for the pinout for the PLD and wire the PLD circuit (with 4 input switches, resistors, and the 7-segment display) on a breadboard. Test the circuit for all input combinations. If it performs correctly, demonstrate it to your instructor.
4. Print the following files from Aldec Active-HDL to include with your report:
 - A) A well-documented VHD file (include many comments).
 - B) A well-documented TestBench file
 - C) A truth table (listing) file - verify that it is correct
 - D) A waveform file – verify that it is correct
 - E) The JEDEC file
 - F) The Chip Report