

## Lab # 6

# Synchronous Counters

### A. Objective

The objective of this laboratory is to introduce the student to synchronous sequential counter circuits designed with JK flip-flops using the excitation table method and to introduce the student to the 74191 synchronous UP/DOWN counter as an example of a commercially available counter.

### B. Materials

Breadboard	7447 and 7-segment display circuit board
5V Power Supply	soldered in earlier lab
7476 Dual JK flip-flops	555 Timer IC
74191 Synchronous UP/DOWN Counter	Assorted resistors and capacitors

### C. Introduction

No new material is introduced in this lab, however, the student may want to review the design of sequential circuits by the “excitation table method” covered in the lecture part of the course. A data sheet for the 74191 is available on the instructor’s web page.

### D. Preliminary Work

1. Design a clock generator using a 555 timer with a frequency of about 1 Hz (any duty cycle is OK). Use resistor values between  $1k\Omega$  and  $1M\Omega$  and use capacitor values available in lab. Show your calculations for  $R_A$ ,  $R_B$ , and  $C$ . Once you have selected standard values to be used for  $R_A$ ,  $R_B$ , and  $C$ , recalculate  $f$ .
2. Design a modified sequence counter that will count out the following sequence: The first four unique digits in your EmplID (not including the digit 9) followed by the digit 9 and then repeat. If you do not have 4 unique digits, then add in as many of the follow digits as you need: 7, 2, 6, 8. Sever examples are shown below.

EmplID	Counting Sequence
2869834	2, 8, 6, 3, 9, and repeat
2662518	2, 6, 5, 1, 9, and repeat
2552525	2, 5, 7, 6, 9, and repeat

Use the excitation table method for your design. Treat unused states as “don’t cares”. Include a switch to initialize the counter to the first count in your sequence.

Your design should include the following:

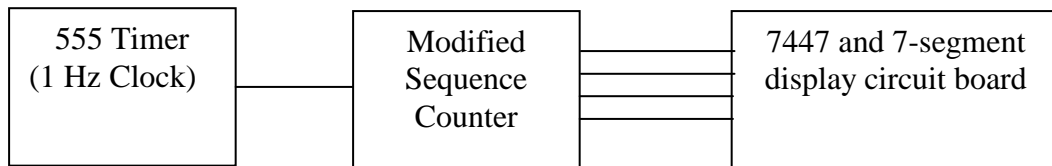
- a state diagram (include only the valid states)
  - a circuit excitation table used to determine JK flip-flop input connections
  - the K-maps used to generate minimal expressions for JK inputs
3. Generate complete circuit documentation for the counter, including a 555 timer circuit designed above, the initialization switch, and the connection of the outputs of the flip-flops to the 7447 and 7-segment display.

A basic block diagram for the circuit to be built and tested is shown below.

4. Generate complete circuit documentation for the connection of a 74191 synchronous UP/DOWN counter, including the clock input, a switch to control the count direction, and the connection of the the 7447 and 7-segment display. Check the data sheet for the 74191 for proper operations of the device (looking at the timing waveforms on the data sheet is particularly useful).

**E. Laboratory Work**

1. Measure and record the resistor and capacitor values to be used for the 1 Hz clock generator. Recalculate the frequency using the measured values and compare it to the designed frequency.
2. Construct the 1 Hz clock generator. Connect an LED and current-limiting resistor to the output to insure that it is working properly (it should blink once per second).
3. Construct the modified sequence counter. Use the 1 Hz clock (remove the LED and resistor from step 1) to clock the counter. Connect the output of the counter to the 7-segment display device. A basic block diagram is shown below. Also add the initialization switch to the circuit. Demonstrate proper operation of the circuit to your instructor.



4. Connect the 74191 synchronous UP/DOWN counter. Use the constructed 1 Hz clock generator to clock the counter. Connect the output of the counter to the 7-segment display device. A basic block diagram is shown below. Demonstrate proper operation of the circuit to your instructor (counting 0 up to 15 and 15 down to 0).

