

## **Test #2 Overview**

Related Homework Assignments: Homework # 3 - 4

Related textbook sections: Chapters 3-4 and Chapter 6, Section 8 on PLAs and PALs in Logic and Computer Design Fundamentals, 4<sup>th</sup> Ed., by Mano

### **Ch. 3 Combinational Logic Design**

Design Procedure:

- Naming the exact steps is not important – just be able to design a circuit
- Design problems – be able to design a custom combinational logic circuit
- Codes will be provided for code converter problems (except you should know the BCD code)

Technology mapping – be able to implement circuits using NAND-only or NOR-only technology

Procedure for implementing a circuit with only NANDs or NORs:

- 1) Draw the AND-OR-NOT circuit
- 2) Replace each gate with the NAND or NOR equivalent
- 3) Cancel back-to-back inverters

BCD-to-7-segment decoders

- common anode versus common cathode
- segment labeling (a-g)
- design of decoder circuit

Other common combinational logic circuits:

- Magnitude Comparators
- Decoders
- Encoders
- Priority Encoders
- Multiplexers
- Demultiplexers

For the devices above:

- Be able to work with active-LOW or active-HIGH inputs, outputs, enable lines, etc.
- Be familiar with the devices as block diagrams or as circuits.
- Be able to design the circuits, extend block diagrams, read or develop truth tables, etc.
- Know what inputs and outputs to expect for a given device.
- Be able to read specification sheets

Implementing Boolean expressions using:

- Decoders (using minterms or maxterms)
- Multiplexers (implementing a function of  $N+1$  variables using a MUX with  $N$  select lines)

### **Ch. 6, Section 8 – Programmable Logic Devices**

Programmable Logic Devices (PLD's)

- General information
- PLAs and PALs
- Implement Boolean expressions using logic array diagrams like Fig. 6-21 and 6-23 in the text

(continued)

**Ch. 4: Arithmetic Functions and HDLs**

Half-adder

Full-adder

N-bit adders

Carry look-ahead circuit (general information)

Representation of negative numbers in 2's complement form

Subtraction using r's complement addition

Subtraction using (r-1)'s complement addition

Signed arithmetic (adding or subtracting signed numbers)

Adder-subtractor circuit

Contraction – modifying an existing circuit or function to create a related (and simpler) circuit or function. Example: Using contraction to form an incrementer from an adder circuit

Given an N-bit adder using full adders, be able to use contraction to form:

- Incrementer
- Increment-by-N circuit

Hardware Description Languages (HDLs)

- Will not be covered on this test
- Our main focus will be using HDL in lab